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10/697,981	10/31/2003	Meir Avraham	246/194	8963

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EXAMINER	
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ART UNIT	**PAPER NUMBER**
2117	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/697,981	AVRAHAM, MEIR	
	Examiner	Art Unit	
	Saqib J. Siddiqui	2117	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 March 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *2,3,5-8,10-23,26-30 and 32-43* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *2,3,5-8,10-23,26-30 and 33-43* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *29 March 2007* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Applicant's response was received and entered March 29, 2007.

- Claims 2-3, 5-8, 10-23, 26-30 and 32-43 are pending.
- Claims 2-3 and 5-6 amended and claims 33-43 are new.
- Application is currently pending.

Response to Amendment

Applicant's arguments and amendments with respect to claims 1-43 filed March 29, 2007 have been considered but they are not persuasive with respect to claims 7-8, 10-17, 23, 30 and. All other arguments are moot under new grounds of rejection.

Applicant puts forth the argument that the prior art of record Chesley US Pat no. 4,333,142, does not teach; loading a testing program into the volatile memory and storing a first testing program for testing said nonvolatile memory. The Examiner respectfully disagrees.

As per the contention that Chesley does not teach loading a test program into the volatile memory Examiner would like to respectfully state that "loading a test program" is a broad limitation that given the write capabilities of RAM it is not possible that the RAM is being tested without any instructions being loaded onto the RAM. Chesley mentions that the module to test the RAM is on the ROM, in order to test the write capabilities of RAM Chesley will have to load some instructions from the ROM, further the address comparator on the RAM will be given an address from the CPU for comparison.

Therefore, it is not possible that Chesley is testing the RAM without loading a testing program onto the RAM.

As per the contention that Chesley does not teach storing a test program on the nonvolatile memory, the Examiner would like to respectfully cite "Each **ROM module contains** an identical copy of a CPU and RAM test program as well as **other desired service routines**, with the addresses shifted to reflect the proper module addresses. In addition, **the last word of each ROM module contains** a check sum of all of the other words of the module so that a CPU can perform a simple test function, in this case summation, upon all words of the ROM to verify that the ROM is operating correctly." Examiner contends that storing a test program on the nonvolatile memory is a broad limitation and the last word of each ROM module, which is used to test the ROM and other desires service routines, which are both contained in the ROM teach a test program being stored on a nonvolatile memory.

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claims 18-22 & 37 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. Claim 18 contains subject matter, which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the

invention. The specification does not enable testing the nonvolatile memory including "writing to said nonvolatile memory."

As per claims 19-22 & 37:

These claims are rejected by virtue of their dependency.

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 23 and 38 rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 23 recites "a nonvolatile memory, fabricated on a first chip, wherein is stored a first testing program." It is not clear if the testing program is stored on the memory or somewhere else on the first chip.

As per claim 38:

This claim is rejected by virtue of its dependency.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claims 2-3, 5, 26-27, 29, 33, 40 and 43 are rejected under 35 U.S.C. 103 (a) as being unpatentable over Chesley US Pat no. 4,333,142 in view of Applicant Admitted Prior Art (AAPA) and further in view of Ledford et al. US Pat no. 6,347,056 B1.

As per claims 26, 29, 33:

Chesley substantially teaches a method of testing an electronic device that includes a CPU (Fig 2 # 22) and at least one memory (Fig 1 # 13), a nonvolatile memory wherein is stored a first testing program (column 3, lines 5-15) comprising the steps of: testing the at least one memory (column 1, lines 40-42), a volatile memory (column 3, lines 15-30) using the CPU (column 1, lines 40-42); and testing the CPU (column 1, lines 42-44) and storing results of said at least one memory in one of said at least one memory by said CPU (column 1, lines 28-37), wherein is stored a first testing program for testing said nonvolatile memory (column 3, lines 7-10); and a volatile memory (Fig 1 # 14), operationally connected to said nonvolatile memory (Fig 1 # 24); and wherein a second program, for testing said volatile memory, is stored in said nonvolatile memory (column 3, lines 47-49) AAPA in an analogous art teaches assembling, fabricating and packaging the CPU and memory in one embodiment (page

1, lines 13-23). It would have been obvious to one of ordinary skill in the art at the time the invention was made to use the method of testing presented in Chesley's invention to test SIP, since one of ordinary skill in the art would have realized that using Chesley's method to test SIP would decrease the duration of testing and reduce the number of testing pins. Further it should be noted that despite the fact that both the CPU and memory are placed on the same chip, it would have been obvious to one of ordinary skill in the art at the time the invention was made to place the CPU on a different chip as that from memory, since it has been held that rearranging parts of an invention involves only routines skill in the art. *In re Japikse,* 86 USPQ 70.

Chesley/AAPA does not explicitly teach storing results of said testing in said nonvolatile memory, by said CPU. However, Ledford et al. in an analogous art teaches storing test results in the non-volatile memory (claim 8). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to enable Chesley/AAPA to store the test results in the non-volatile memory because Chesley/AAPA mention saving data in other suitable medium. "Data indicating the condition of the RAM's is stored in a table formed in the CPU registers or in one of the RAM's or in another suitable store." (column 1, lines 38-47). Here again the non volatile memory is the ROM and the volatile memory is the RAM, whose test results can be stored in the CPU registers, or in "another suitable store." Within the context of Chesley "suitable store" can be interpreted to be the ROM because these are the only three memory components in the prior art and it would be advantageous to store the results in the ROM to prevent data loss upon a power failure. Further, Examiner would like to

contend that the use of RAM and ROM is only a preferred embodiment in Chesley and Chesley can be modified to test any kind of volatile and non-volatile memory within the scope of Chesley's claims. Support for this contention can be found in the claims of Chesley, where ROM and RAM are not mentioned in fact Chesley's claims teach the testing of memory chips using a CPU. The Supreme Court has held that "a patent for a combination which only unites old elements with no change in their respective functions...obviously withdraws what is already known into the field of its monopoly and diminishes resources available to skillful men...The combination of familiar elements according to known methods is likely to be obvious when it does no more than yield predictable results." *KSR Int'l Co. v. Teleflex Inc., 2007 U.S. LEXIS 4745*, (U.S. 2007)

As per claim 2:

Chesley/AAPA/Ledford teaches the method wherein said testing of the CPU is effected subsequent to said testing of the at least one memory (column 3, lines 37-39).

As per claims 3 and 34:

Chesley/AAPA/Ledford teaches the method further comprising the step of: loading a testing program into one of said at least one memory (Fig 3, # 27, column 3, lines 1-2), the CPU then testing at least one of said at least one memory by executing said testing program (column 3, lines 2-6).

As per claim 5:

Chesley/AAPA/Ledford teaches the method; wherein said testing of the CPU includes reading said stored results from said one of said at least one memory (column 3, lines 37-39).

As per claim 27:

Chesley/AAPA/Ledford teaches the method further comprising the steps of: executing a second testing program in order to test the nonvolatile memory (column 3, lines 10-16); and (d) storing results of said executing of said second testing program in the nonvolatile memory (column 3, lines 30-45).

As per claims 40 and 43:

Chesley/AAPA/Ledford teach the device and method as rejected above, wherein a single said CPU is fabricated on said third chip (Chesley claim 3).

Claims 7-8, 10-16, 18-21, 23, 30, 32, 36-39 and 41-42 are rejected under 35 U.S.C. 103 (a) as being unpatentable over Chesley US Pat no. 4,333,142 in view of Applicant Admitted Prior Art (AAPA)

As per claim 7:

Chesley substantially teaches a method of testing an electronic device that includes a CPU (Fig 2 # 22) and at least one memory (Fig 1 # 13), comprising the steps of: testing the at least one memory (column 1, lines 40-42), loading a testing program into said volatile memory, using the CPU to execute said testing program (column 1, lines 40-42); and testing the CPU (column 1, lines 42-44).

Chesley does not explicitly teach the method of assembling the CPU and memory on separate chips.

However, AAPA in an analogous art teaches assembling, fabricating and packaging the CPU and memory in one embodiment (page 1, lines 13-23). It would

have been obvious to one of ordinary skill in the art at the time the invention was made to use the method of testing presented in Chesley's invention to test SIP, since one of ordinary skill in the art would have realized that using Chesley's method to test SIP would decrease the duration of testing and reduce the number of testing pins. Further it should be noted that despite the fact that both the CPU and memory are placed on the same chip, it would have been obvious to one of ordinary skill in the art at the time the invention was made to place the CPU on a different chip as that from memory, since it has been held that rearranging parts of an invention involves only routines skill in the art. *In re Japikse,* 86 USPQ 70.

As per claim 8:

Chesley/AAPA teaches the method wherein said testing of the CPU is effected subsequent to said testing of the at least one memory (column 3, lines 37-39).

As per claim 10:

Chesley/AAPA teaches the method further comprising the step of: storing said testing program in the nonvolatile memory (column 3, lines 7-10), said loading of the testing program into the volatile memory then being from the nonvolatile memory (column 3, lines 47-49).

As per claim 11:

Chesley/AAPA teaches the method wherein said loading of the testing program from the nonvolatile memory to the volatile memory is effected by the CPU (column 3, lines 47-49).

As per claim 12:

Chesley/AAPA teaches the method further comprising the step of: storing results of said testing in the nonvolatile memory, by the CPU (Figure 2 # 28, column 3, lines 49-54).

As per claim 13:

Chesley/AAPA teaches the method wherein said testing of the CPU includes reading said stored results from said nonvolatile memory (column 3, lines 55-60).

As per claim 14:

Chesley/AAPA teaches the method further comprising the step of: storing a testing program in the nonvolatile memory (column 3, lines 7-10), the CPU then testing at least one of the memories by executing said testing program directly in said nonvolatile memory (column 3, lines 10-16).

As per claim 15:

Chesley/AAPA teaches the method of claim 14, further comprising the step of: storing results of said testing in the nonvolatile memory, by the CPU (column 3, lines 30-37).

As per claim 16:

Chesley/AAPA teaches the method, wherein said testing of the CPU includes reading said stored results from said nonvolatile memory (column 3, lines 37-46).

As per claim 36:

Chesley/AAPA teach the method as rejected above, wherein a single said CPU is fabricated on said third chip (Chesley claim 3).

As per claim 18:

Chesley substantially teaches a method of testing an electronic device that includes a CPU (Fig 2 # 22) and at least one memory (Fig 1 # 13), comprising the steps of: testing the at least one memory (column 1, lines 40-42), using the CPU (column 1, lines 40-42); and testing the CPU (column 1, lines 42-44) storing in the said nonvolatile memory a program for testing said nonvolatile memory by steps including writing to said nonvolatile memory (the test pattern was written into the ROM, initially).

Chesley does not explicitly teach the method of assembling the CPU and memory on separate chips.

However, AAPA in an analogous art teaches assembling, fabricating and packaging the CPU and memory in one embodiment (page 1, lines 13-23). It would have been obvious to one of ordinary skill in the art at the time the invention was made to use the method of testing presented in Chesley's invention to test SIP, since one of ordinary skill in the art would have realized that using Chesley's method to test SIP would decrease the duration of testing and reduce the number of testing pins. Further it should be noted that despite the fact that both the CPU and memory are placed on the same chip, it would have been obvious to one of ordinary skill in the art at the time the invention was made to place the CPU on a different chip as that from memory, since it has been held that rearranging parts of an invention involves only routines skill in the art. *In re Japikse,* 86 USPQ 70.

As per claim 19:

Chesley/AAPA teaches the method, further comprising the step-of: loading said testing program from the nonvolatile memory into a volatile memory, said executing of said testing program then being from said volatile memory (column 3, lines 46-49).

As per claim 20:

Chesley/AAPA teaches the method further comprising the step of: including said volatile memory in the system-in-package (Fig 1 #14).

As per claim 21:

Chesley/AAPA teaches the method, further comprising the step of: storing results of said executing in the nonvolatile memory (Figure 2 # 28, column 3, lines 49-54).

As per claim 37:

Chesley/AAPA teach the method as rejected above, wherein a single said CPU is included in system in package (AAPA).

As per claim 23:

Chesley substantially teaches an electronic device comprising: a nonvolatile memory (Fig 1 # 13), wherein is stored a first testing program for testing said nonvolatile memory (column 3, lines 7-10); and a volatile memory (Fig 1 # 14), operationally connected to said nonvolatile memory (Fig 1 # 24); and wherein a second program, for testing said volatile memory, is stored in said nonvolatile memory (column 3, lines 47-49).

Chesley does not explicitly teach the method of assembling the CPU and memory on separate chips.

However, AAPA in an analogous art teaches assembling, fabricating and packaging the CPU and memory in one embodiment (page 1, lines 13-23). It would have been obvious to one of ordinary skill in the art at the time the invention was made to use the method of testing presented in Chesley's invention to test SIP, since one of ordinary skill in the art would have realized that using Chesley's method to test SIP would decrease the duration of testing and reduce the number of testing pins. Further it should be noted that despite the fact that both the CPU and memory are placed on the same chip, it would have been obvious to one of ordinary skill in the art at the time the invention was made to place the CPU on a different chip as that from memory, since it has been held that rearranging parts of an invention involves only routines skill in the art. *In re Japikse,* 86 USPQ 70.

As per claims 30 and 32:

These claims are rejected under similar grounds as above.

As per claim 38:

Chesley/AAPA teach the device as rejected above, wherein a single said CPU is fabricated on said third chip (Chesley claim 3).

As per claims 39 and 41-42:

These claims are rejected under similar grounds as above.

Claims 6, 17, 22, 28 and 35 are rejected under 35 U.S.C. 103(a) as being unpatentable Chesley/AAPA/Ledford and further in view of Takizawa US Pat no. 6198663 B1

As per claim 6:

Chesley/AAPA/Ledford substantially teaches a method of testing an electronic device that includes a CPU (Fig 2 # 22) and at least one memory (Fig 1 # 13), comprising the steps of: (a) testing the at least one memory (column 1, lines 40-42), using the CPU (column 1, lines 40-42); and b) testing the CPU (column 1, lines 42-44).

Chesley/AAPA/Ledford does not explicitly teach teaches the method, wherein said testing of said at least one memory is effected during a burn-in of the electronic device.

However, Takizawa in an analogous art teaches the method, wherein said testing of said at least one memory is effected during a burn-in of the electronic device (Figure 1 # 61a, column 4, lines 34-47). Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to execute testing during a burn-in of the electronic device, since one of ordinary skill in the art would have recognized that executing testing during a burn-in would have assisted in stabilizing outputs, and identifying early life failures normally resulting from thermal or other effects.

As per claims 17, 22, 28 and 35:

Rejected based on the same argument as claim 6.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Saqib J. Siddiqui whose telephone number is (571) 272-6553. The examiner can normally be reached on 8:00 to 4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jacques Louis-Jacques can be reached on (571) 272-6962. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Saqib Siddiqui
Art Unit 2138
06/05/2007

GUY LAMARRE
PRIMARY EXAMINER